AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 12, lines 1-30 with the following amended paragraph.

The page register 140 in this preferred embodiment incorporates bit sprinkling functionality to maximize the physical spacing between bits in a given oct-byte and, accordingly, to improve the effectiveness of the ECC protection. Further details on the bit sprinkling functionality can be found in "Memory Device and Method for Storing Bits in Non-Adjacent Storage Locations in a Memory Array," U.S. patent application serial no. 10/024,647 ~~(attorney docket no. 10519/60; filed on the same day as the present application)~~, which is assigned to the assignee of the present application and is hereby incorporated by reference. While control logic is responsible for physically mapping a page into the memory array 150, data scrambling and de-scrambling in the sub-registers is enabled as a hardware feature of the page register 140 and is transparent to the control logic. Further, the SMI logic will see the data in its original form at all times. Figure 8 is an illustration of the page sub-register for bay 0. One byte of each word in the page is stored in the page sub-register from top to bottom. For example, bits A0-A7 of ECC word A are stored in rows 0-7 of the first column, bits B0-B7 of ECC word B are stored in rows 0-7 of the second column, etc. When bits are read out of the page sub-register and into a corresponding sub-array, the bits are read from left to right (*e.g.*, A0 B0 C0 . . . H0). The bits read from the page sub-register are then stored in the corresponding sub-array, as illustrated in Figure 9. (Addressing of the columns is taken care of by the column decoders in the array.) As shown in Figure 9, because the direction that the bits were stored in the page sub-register is

different from the direction that the bits were read out of the page sub-register, bits in an ECC word are located in non-adjacent locations in the memory array. Specifically, each bit is 64 storage locations apart in the sub-array (*e.g.*, A0 is 64 storage locations apart from A1), thereby achieving maximum separation between bits of an oct-byte. Accordingly, a local manufacturing defect must be large enough to extend across 65 bit locations before causing a double-bit error within an ECC word. A defect that extends across 64 bits locations will only result in a correctable single-bit error in 64 ECC words, instead of an uncorrectable multi-bit error in a single ECC word. This enhances the yield and reliability of the memory device 100 with a minimal amount of overhead and implementation cost. The same principles described above apply to storage of the ECC syndrome bits in the sub-array in bay 4.

Please replace the paragraph on page 13, lines 1-17 with the following amended paragraph.

As discussed above, the spare array in Bay 9 is physically made up of two ¼-sized sub-arrays that logically act as a single array of 1024 rows and 512 columns (excluding redundancy and sacrificial test areas). To enable maximum separation between bits of an oct-byte in the spare array, bits are sprinkled within the page register 140. To simplify the interface between the page register 140 and the control logic, each page sub-register preferably is extended to hold a section of the spare array data as shown in Figure 10. The addition extends the sub-register by another bit (from eight to nine) for half of its height. As the page register 140 is made of nine sub-registers, the spare array data will be contained within the extended sections of these sub-registers as shown in Figure 11. In Figure 11, each block represents one byte of data (one bit wide and eight bits deep). SP0 and SP1 are the spare array data (16-bytes) and ECC0 and ECC1 are their respective ECC syndrome bits. XY is used to store redundancy/self-repair data. R is a reserved area, which can be used to store dynamic bit inversion information, as described in "Memory Device and Method for Dynamic Bit Inversion," U.S. patent application serial no. 10/023,466 ~~——— (attorney docket no. 10519/64; filed on the same day as the present application)~~, which is assigned to the assignee of the present application and is hereby incorporated by reference. XYM and RM are masked bit locations in XY and R space.